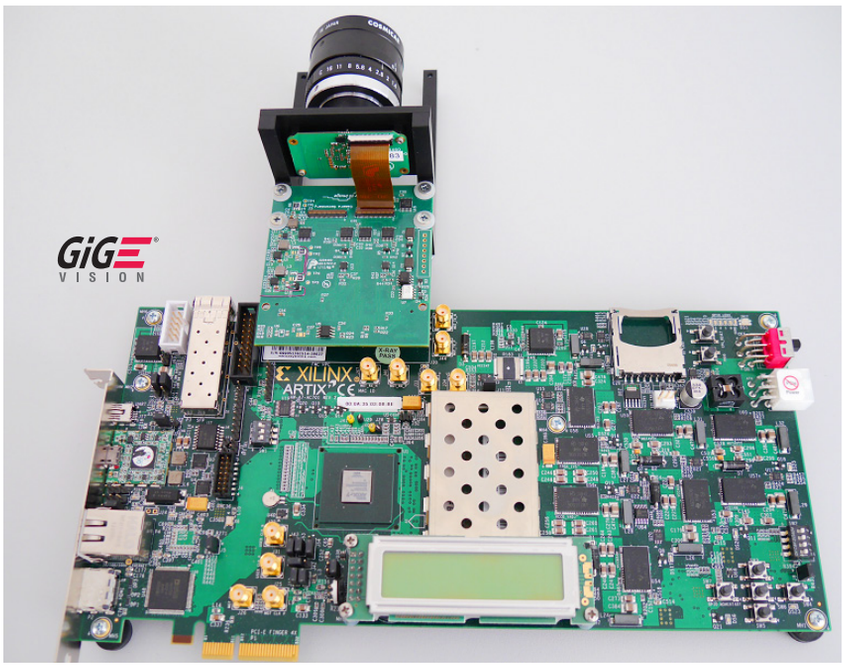
IMXDK - Sony IMX® CMOS Sensor Kit

Development kit for Sony IMX® CMOS sensor with FPGA

FPGA on ALTERA or XILINX vendor hardware

With IMXDK we have, for the first time, all Sony IMX® CMOS sensors on one open platform to test:

- **IMX type A: IMX174, 249**
- **IMX type B: IMX250*, 252, 253*, 255 , 264*, 265*, 267**
- **IMX type C: IMX273***
- **IMX type D: IMX287**
- **FPGA core on Artix7, Cyclone5, Kintex7 and ARRIA FPGA**



IMXDK Evaluation System

IMX - FPGA Core

Is an open and prebuilt platform to evaluate sensors and design cameras in the same environment as thex prevail when the cameras will be in production. You can run the sensor in your native FPGA fabric with full speed timing and sensor readout, add and use all available debug tools from the FPGA vendors to analyse and debug sensor data, add your own image data pipeline and finally send the image data to a PC with GigE Vision®, USB3 Vision® and CoaXPress® to do even deeper analyses of the sensor data or start immediately your full camera design.

Design

The base for the sensor FPGA IP is a FMC PCB, which forms the interface between the sensor and a standard FPGA evaluation card from a FPGA vendor. The FMC card is designed to be FMC-LPC compliant and does all needed power and level adoptions for the IMX CMOS sensor. Known cards to work with the FMC are ALTERA® Altera Arria V GT FPGA Development Kit, XILINX® Artix-7 FPGA AC701 Evaluation Kit and Kintex-7 FPGA KC705 Evaluation Kit.

Especially useful are the Arria5 and KC705 kits, as they have 2 FMC connectors, so that the second connector can be used for another U3V or CXP interface card. GigEVision at 1GBit is available on all commonly used FPGA kits.

Delivery

The core is availabe in plain C and encrypted VHDL sources with and without production royalties. The C part of the core takes care of the sensor configuration while the VHDL part is responsible for timing and readout of the sensor data.
The C code can be easily expanded and adapted to your needs, while we want to keep the VHDL closed and optimized to deliver full speed in all supported FPGAs.

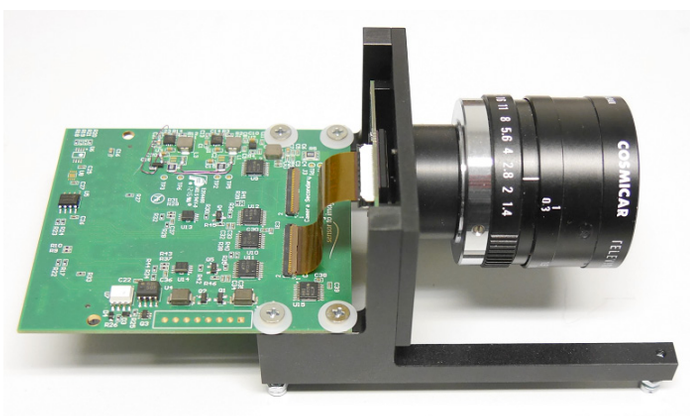
All S2I IP on IMXVDK is available in a 30min time bombed variant with downloadable VIVADO based design on AC701. All designs include a step-by-step tutorial and are ready to go within a few minutes.

FPGA RESOURCES

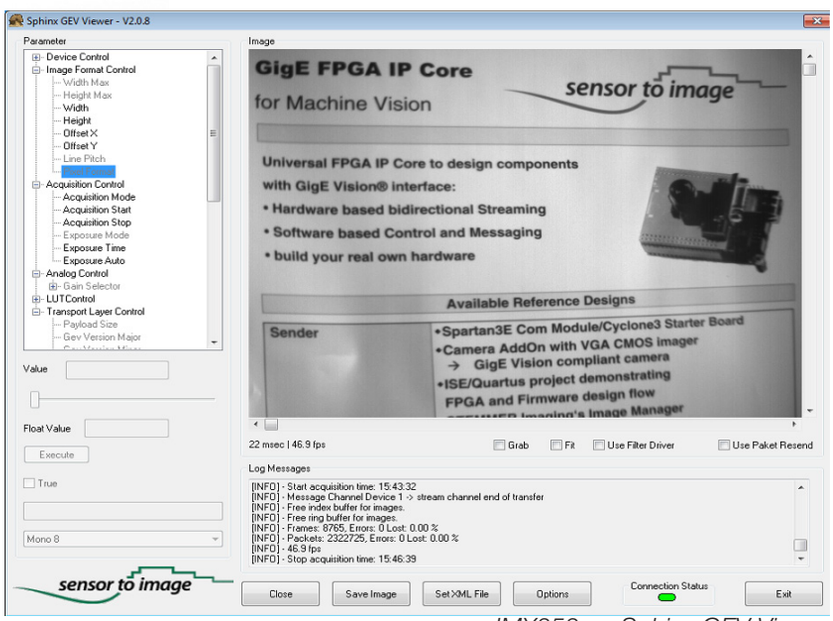
MODULE	IMX174, 249	IMX 252, 255	IMX273	IMX287
FPGA serial LVDS read out				
– Slice registers	1237	678/1227/2271	tbd	tbd
– Slice lookup tables, no BRAM used	805	596/836/1558	tbd	tbd
– Sensor read-out LBDS lanes	8	4/8/16	tbd	tbd
– Minimum LVDS readout frequency for full read out speed	297 MHz	297 MHz	tbd	tbd
FPGA control interface and timing generator				
– Slice registers	745	755	tbd	tbd
– Slice lookup tables	592	587	tbd	tbd
– Block RAMs	0	0	tbd	tbd
– Maximum sensor clock frequency	195 MHz	195 MHz	tbd	tbd
MicroBlaze based control protocol implementation				
– Slice registers	4750	4750	4750	4750
– Slice lookup tables	4264	4264	4264	4264
– BlockRAMs	16	16	16	16
– Maximum AXI clock frequency to IMX control interface	277MHz	277 MHz	tbd	tbd
– Minimum CPU clock frequency	62.5 MHz	62.5 MHz	62.5 MHz	62.5 MHz

values are post synthesize only and based on ARTIX7, other architectures might have different resource usage

tbd: has still to be designed in future.



FMC and IMX174 sensor



IMX252 on Sphinx GEV Viewer

Sensor to Image GmbH
Lechtorstraße 20
86956 Schongau · Germany
Phone: +49 8861 2369-0
Fax: +49 8861 2369-69
email@sensor-to-image.de

* = Preliminary data. Subject to change.